REMARKS

The present application contains claims 5-8, 17, 18, and 21-27. Claims 21-27 have been newly added and claims 5-8, 17 and 18 have been amended to more clearly distinguish over the art of record.

Making reference to the detailed action, it is noted that the allowability of claims 5-8, 17 and 18 has been withdrawn.

Responsive to the claim objections, claims 17 and 18 have been amended to change "method" to "apparatus" to conform with amended claim 5.

Claims 5-8 and 18 have been rejected under 35 U.S.C. § 103(a) as unpatentable under over Lee '199 in view of Ando '932. This rejection is respectfully traversed as regards claims 5-8 and 18, as amended.

As amended, main claim 5 positively recites a first correlator for determining a correlation between said sequence and a stored sequence and a second correlator for determining correlation between said sequence and the stored sequence which has been altered in phase.

Lee fails to teach or even remotely suggest first and second correlators for respectively determining a correlation between the sequence and a stored sequence, and for determining a correlation between a sequence and the stored sequence which has been altered in phase. Figure 2 of '199 is limited to a single correlation

unit 251. Also there is no teaching of applying the stored sequence, i.e. the sequence derived from PSC generator 252 shown in Figure 2 of '199 and applying it to the first correlator, then a second correlator after the output of PSC generator 252 has been altered in phase.

Although Figure 5 of '199 teaches a plurality of correlation units 500, 510 and 520, which are described as "partial correlation units", the detailed operation of the block diagram of Figure 5 set forth in paragraph [0036] states that each of the partial correlation units 500, 510 and 520 divides the SCH of a 256-chip length in each slot into M blocks with respect to the output SCH of the ADC 240 and partially correlates the complex conjugate of the PSC generated by generator 252 with the M blocks of the SCH. There is neither teaching or remote suggestion of applying the 256-chip PSC to two different correlators at two different phases.

Making reference to Ando '932, this patent is limited to teaching a phase locked loop (PLL) circuit. Even assuming, for the sake of argument, that Ando '932 is combinable with Lee '199 in the manner proposed by the examiner, there is nevertheless no teaching in either of these two references, taken either alone or in combination, of the novel features mentioned above, namely determining a correlation between a sequence and a stored sequence at a first correlator and determining a correlation between the sequence and the stored sequence which has been altered in phase at a second correlator. In view of the forgoing comments, it is

submitted that claim 5 patentably distinguishes over the combination of Lee '199 in view of Ando '932.

Claims 6-8 and 18 depend from claim 5 and carry all of its limitations and hence are deemed to patentably distinguish over Lee '199 and Ando '932 for the same reasons set forth above regarding claim 5.

Claims 7 and 8 have been rejected under 35 U.S.C. § 103(a) as unpatentable over Lee '199 and Ando '932 as applied to claim 5 and further in view of Patapoutian '343. This rejection is respectfully traversed.

In view of the fact that claims 7 and 8 depend from claim 5 and hence carry all its limitations, it is submitted that claims 7 and 8 patentably distinguish over the combination of Lee '199 and Ando '932 for the same reasons set forth here and above in regard to claim 5.

The examiner has relied upon Patapoutian '343 for teaching a filter that is a proportional integral (PI) filter.

Patapoutian '343 is limited to teaching a PI filter and, even assuming, for the sake of argument, that Patapoutian '343 is combinable with Lee '199 and Ando '932 in a matter suggested by the examiner, Patapoutian, like Ando, is lacking in the same features lacking in Lee, namely determining the correlation of a sequence with a stored sequence at a first correlator and determining a correlation between the given sequence and the stored sequence which has been altered in phase. In

view of the forgoing comments, it is submitted that claims 7 and 8 patentably distinguish over the combination of Lee '199, Ando '932 and Patapoutian '343.

New claims 21-26 all depend from claim 5 and carry all of its limitations and hence are deemed to patentably distinguish over Lee '199, Ando '932 and Patapoutian '343 references, taken either alone or in combination, for the same reasons set forth above with regard to claim 5.

Claim 21 further recites a Step 1 processing means which *periodically* processes a synchronization code in a primary synchronization channel to provide location updates. These features are neither taught nor remotely suggested by the above-identified references. Claim 22 depends from claim 5 and further recites the error estimator as further comprising means for providing first, second and third frequency estimates and means for averaging the first, second and third frequency estimates. Claim 23 depends from claim 22 and recites the first, second and third frequency estimates as being early, punctual and late estimates. Claim 24 depends from claim 22 and recites means for providing early, punctual and late frequency estimates which include means to provide an early offset estimate which is $-\frac{1}{2}T_C$ relative to the punctual offset and means to provide a late offset which is $+\frac{1}{2}T_C$ relative to the punctual offset where T_C is no greater than ½ of a sampling rate.

Claim 25 depends from claim 5 and recites first means for applying a positive phase rotation to the stored sequence and second means for applying a negative rotation to the stored sequences.

Claim 26 depends from claim 25 and recites the first and second means rotate the stored sequence at the same frequency. These features are neither taught nor remotely suggested by the cited prior art.

New claim 27 recites apparatus for performing start up automatic frequency control (AFC) during an initial cell search (ICS) by a user equipment receiver comprising:

means for performing Step 1 processing of a received code sequence to provide a location of a synchronization channel;

a sequence locator and splitter responsive to a location output of said Step 1 processing means for producing early, punctual and late frequency offsets based on the received sequence;

first, second and third frequency estimators respectively determining an estimated frequency from said early, punctual and late offsets;

means for averaging the estimated frequencies;

a filter for selectively integrating the error estimate; and

one of a voltage control isolator (VCO) and a numeric controlled isolator (NCO) for adjusting frequency of the receiver responsive to the integrated error estimate.

These features are neither taught nor remotely suggested in Lee '199, Ando '932 and Patapoutian '343, taken either alone or in combination. It is therefore submitted that claims 21-27 patentably distinguish over the art of record.

In view of the forgoing comments, it is submitted that claims 5-8, 17 and 18 patentably distinguish over the art of record and reconsideration and allowance of these claims are earnestly solicited and that new claims 21-27 patentably distinguish over the art of record and consideration and allowance of these claims is likewise earnestly solicited.

Respectfully submitted,

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